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VALENTIN, JUAN D	
ART UNIT	PAPER NUMBER
2877	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,156	STIRTON, JAMES BROC	
	Examiner	Art Unit	
	Juan D Valentin II	2877	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1-37 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Singh et al. (USPUB 20020135781, hereinafter Singh).

Claim 1

Singh discloses a method comprising of providing a semiconductor substrate and forming a first plurality of implant regions (features) in a said substrate (abstract). Singh further discloses illuminating said first plurality of implant regions with a light source in a scatterometry tool where said scatterometry tool generates a trace (feature) profile corresponding to an implant profile of said implant regions (abstract).

Claim 2

Singh discloses a method further comprising generating an additional trace profile for an additional plurality of implant regions formed in said substrate or additional substrates. The said additional plurality of implant regions having an implant profile different from said first plurality of implant regions (pg. 2, 0012).

Claim 3

Singh further discloses a method further comprising a library (database) comprised of a plurality of calculated trace profiles of implant regions having varying implant profiles (pg. 2, 0012 and 0013).

Claim 4

Singh further comprises a method wherein said first plurality of implant regions in said substrate comprises forming a first plurality of implant regions to thereby define a grating structure in said substrate (pg. 1, 0010).

Claim 5

Singh further discloses a method wherein said first plurality of implant regions are comprised of N-type dopant material or P-type dopant material (pg. 6, 0059). It is inherent and well known to someone of ordinary skill in the art that a semiconductor substrate with implant regions or features are going to be doped with either a P-type or N-type dopant. Applicant is appreciated that the reference of Singh reads upon the claimed limitations.

Claim 6

Singh further discloses wherein first plurality of implant regions are illuminated using at least one of a multiple wavelength light source and a single wavelength light source (pg. 2, 0012).

Claim 7

Singh further discloses a method wherein said implant profile is comprised of at least one of a width, a depth, a dopant concentration level, and a dopant concentration profile of said implant regions (pg. 6, 0062 and 0065). It is inherent and well known to someone of ordinary

skill in the art that a variety of different substrate features can be altered in order to create different databases of process profiles. Applicant is appreciated that the reference of Singh reads upon the claimed limitations.

Claim 8

Singh discloses a method of measuring profiles of implant regions formed in a semiconductor substrate comprising forming a plurality of implant regions in a semiconductor substrate and illuminating said plurality of implant regions (abstract). Singh further discloses measuring light reflected off the substrate to generate a profile trace for said implant regions and then comparing the generated profile trace to a target profile trace (abstract). Singh further discloses modifying based upon a deviation between the generated profile trace and the target profile trace at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (pg. 2, 0029).

Claim 9

Singh further discloses a method comprising correlating the generated profile trace to a profile trace from a library where the profile trace from the library has an associated implant region profile (pg. 2, 0012).

Claim 10

Singh further discloses modifying based upon a deviation between the generated profile trace and the profile trace from the library, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (pg. 2, 0029).

Claim 11

Singh further discloses a method wherein measuring the reflected light comprises measuring the intensity of the reflected light (pg. 3, 0032).

Claim 12

Singh further discloses a method comprising providing a library of calculated profiles traces, each of which correspond to a unique profile of an implanted region (pg. 2, 0012 and 0029). Singh discloses saving generated profiles for future use and also discloses correlating generated profiles against known profiles in a database. Therefore, it is the position of the Office that the reference of Singh reads upon the applicants claimed limitations.

Claim 13

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone after the profile has been generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 14

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well

known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone prior to the profile being generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 15

Singh discloses a method wherein modifying at least one parameter of an ion implant process comprises modifying at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (pg. 1, 0005). It is inherent and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in order to quickly optimize production of the semiconductor devices. Therefore, applicant will be appreciated that the reference of Singh reads on the applicants claimed limitations.

Claim 16

Singh discloses a method of measuring profiles of implant regions formed in a semiconductor substrate comprising forming a plurality of implant regions in a semiconductor substrate and illuminating the said plurality of implant regions (abstract). Singh further discloses measuring light reflected off the substrate to generate a profile trace for said implant regions and then comparing the generated profile trace to a calculated profile trace in a library where the calculated profile trace has an associated implant region profile (pg. 2, 0012 and 0013). Singh further discloses modifying based upon said comparison of the generated profile trace and the

calculated profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates (pg. 2, 0012 and 0013).

Claim 17

Singh discloses a method further comprising the generated profile trace to a target profile trace from said library (pg. 2, 0012).

Claim 18

Singh further discloses a method of modifying based upon a comparison of the generated profile trace and the target profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (pg. 2, 0029).

Claim 19

Singh further discloses a method wherein measuring the reflected light comprises measuring the intensity of the reflected light (pg. 3, 0032).

Claim 20

Singh further discloses a method comprising providing a library of calculated profiles traces in a library, each of which correspond to a unique profile of an implanted region (pg. 2, 0012 and 0029). Singh discloses saving generated profiles for future use and also discloses correlating generated profiles against known profiles in a database. Therefore, it is the position of the Office that the reference of Singh reads upon the applicants claimed limitations.

Claim 21

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well

known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone after the profile has been generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 22

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone prior to the profile being generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 23

Singh discloses a method wherein modifying at least one parameter of an ion implant process comprises modifying at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (pg. 1, 0005). It is inherent and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in order to quickly optimize production of the

semiconductor devices. Therefore, applicant will be appreciated that the reference of Singh reads on the applicants claimed limitations.

Claim 24

Singh discloses a method of measuring profiles of implant regions formed in a semiconductor substrate comprising forming a plurality of implant regions in a semiconducting substrate and illuminating said plurality of implant regions (abstract). Measuring light reflected off the substrate to generate a profile trace for said implant regions (pg. 2, 0012). Providing a library comprised of a plurality of calculated profile traces, each of which corresponds to a unique profile of an implanted region and further comparing the generated profile trace to at least one of said calculated profile traces from said library (pg. 2, 0012 and 0029). Singh further discloses modifying based upon said comparison of the generated profile trace and the calculated profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates (pg. 2, 0012 and 0013).

Claim 25

Singh further discloses a method comprising the generated profile trace to a target profile trace (abstract).

Claim 26

Singh further discloses modifying based upon a deviation between the generated profile trace and the target profile trace, at least one parameter of an ion implantation process used to form implant regions on subsequently processed substrates (pg. 2, 0029).

Claim 27

Singh further discloses a method wherein measuring the reflected light comprises measuring the intensity of the reflected light (pg. 3, 0032).

Claim 28

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone after the profile has been generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 29

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone prior to the profile being generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 30

Singh discloses a method wherein modifying at least one parameter of an ion implant process comprises modifying at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (pg. 1, 0005). It is inherent and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in order to quickly optimize production of the semiconductor devices. Therefore, applicant will be appreciated that the reference of Singh reads on the applicants claimed limitations.

Claim 31

Singh discloses a method of measuring profiles of implant regions formed in a semiconductor substrate comprising forming a plurality of implant regions in a semiconducting substrate and illuminating said plurality of implant regions (abstract). Measuring light reflected off the substrate to generate a profile trace for said implant regions and comparing the generated profile trace to a target profile trace (pg. 2, 0012). Singh further discloses modifying based upon said comparison of the generated profile trace and the calculated profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates (pg. 2, 0012 and 0013). Singh discloses said at least one parameter comprises at least one of an ion implant energy, an implant angle, a dopant material, and a dopant material concentration (pg. 1, 0005). It is inherent and well known to someone of ordinary skill in the art that during the fabrication process of semiconductor devices, certain process parameters such as implant angles, dopant material and dopant material concentration among others are variable in

order to quickly optimize production of the semiconductor devices. Therefore, applicant will be appreciated that the reference of Singh reads on the applicants claimed limitations.

Claim 32

Singh further discloses a method comprising comparing the generated profile trace to a calculated profile trace in a library where the calculated profile trace has an associated implant region profile (pg. 2, 0012).

Claim 33

Singh further discloses modifying based upon said comparison of the generated profile trace and the calculated profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates (pg. 2, 0012 and 0013).

Claim 34

Singh further discloses a method wherein measuring the reflected light comprises measuring the intensity of the reflected light (pg. 3, 0032).

Claim 35

Singh further discloses a method comprising providing a library of historical profile traces, each of which correspond to a unique profile of an implanted region (pg. 2, 0012 and 0029).

Claim 36

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a

functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone after the profile has been generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Claim 37

Singh further discloses a method wherein measuring light reflected off the substrate to generate a profile trace for said implant regions is performed prior to the implanted regions being subjected to an annealing process or a diffusion process (pg. 1, 003). It is inherent and well known to someone of ordinary skill in the art that the baking step disclosed by Singh is a functional equivalent to an annealing process. In light of the disclosure of Singh, the process disclosed is repeated repetitively until all features have been formed, it is held that the said annealing process can be undergone prior to the profile being generated. Therefore, applicant will be appreciated that the reference of Singh reads upon the claimed limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan D Valentin II whose telephone number is (703) 605-4226. The examiner can normally be reached on M-Th., Every other Fr..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (703) 308-4881. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308- 0955.

Juan D. Valentin, II
Examiner - 2877

Michael P. Stafira
Primary Patent Examiner
Technology Center 2800

JDV
December 20, 2002